## AMENDMENTS TO THE CLAIMS

Claim 1 (currently amended): A power amplifier integrated circuit comprising:

a substrate;

a heat sink for dissipating heat;

a transistor ~~disposed~~ integrally formed on the substrate, the transistor comprising a collector, a base, and at least an emitter; and

an emitter electrode directly connecting the heat sink and the emitter.

Claim 2 (original): The power amplifier integrated circuit of claim 1 wherein the transistor is a heterojunction bipolar transistor (HBT).

Claim 3 (original): The power amplifier integrated circuit of claim 1 wherein the emitter comprises a metallization layer.

Claim 4 (original): The power amplifier integrated circuit of claim 1 wherein the emitter electrode is a flip-chip bump.

Claim 5 (original): The power amplifier integrated circuit of claim 4 wherein the heat sink and the substrate sandwich the transistor.

Claim 6 (original): The power amplifier integrated circuit of claim 1 wherein the emitter electrode is a backside via penetrating the substrate.

Claim 7 (original): The power amplifier integrated circuit of claim 6 wherein the heat sink and the transistor sandwich the substrate.

Claim 8 (original): The power amplifier integrated circuit of claim 1 comprising more than one emitter, and emitters are mutually connected by a metallization layer.

Claim 9 (original): The power amplifier integrated circuit of claim 1 wherein the

emitter electrode and the heat sink provide an electrical ground connection to the emitter.

Claim 10 (original): The power amplifier integrated circuit of claim 1 wherein the heat sink is a metal layer.

Claim 11 (original): The power amplifier integrated circuit of claim 1 wherein a plurality of transistors and a plurality of emitter electrodes are disposed in an array, and operate as a functional device.

Claim 12 (original): The power amplifier integrated circuit of claim 1 wherein th substrate is a GaAs substrate.

Claim 13 (currently amended): A method for manufacturing a heat dissipating power amplifier integrated circuit, the method comprising:

providing a substrate;

providing a heat sink for dissipating heat;

integrally forming a transistor on the substrate, the transistor comprising a collector, a base, and at least an emitter; and

directly connecting the heat sink and the emitter using an emitter electrode.

Claim 14 (original): The method of claim 13 wherein forming the transistor comprises:

disposing a metallization layer on the substrate to form the emitter; and

disposing a second metallization layer to mutually connect emitters.

Claim 15 (original): The method of claim 13 further comprising:

electrically grounding the emitter through the emitter electrode and the heat sink.

Claim 16 (original): The method of claim 13 further comprising:

arraying a plurality of transistors and a plurality of emitter electrodes to

form a functional device.

Claim 17 (currently amended): A power amplifier integrated circuit comprising:

a substrate;

an electrically conductive layer;

a transistor integrally formed on the substrate, the transistor comprising a collector, a base, and an emitter; and

a bump directly disposed on the emitter so as to connect the emitter with the electrically conductive layer for heat dissipation.

Claim 18 (original): The power amplifier integrated circuit of claim 17 wherein the electrically conductive layer and the substrate sandwich the transistor.

Claim 19 (original): The power amplifier integrated circuit of claim 17 wherein the electrically conductive layer provides an electrical ground connection to the emitter.

Claim 20 (original): The power amplifier integrated circuit of claim 17 wherein the electrically conductive layer is a metal layer.

Claim 21 (previously presented): A power amplifier integrated circuit comprising:

a substrate;

a transistor disposed on the substrate, the transistor including a collector, a base, and an emitter, the emitter including an enlarged portion located laterally away from the collector and the base;

a heat sink for dissipating heat; and

a flip-chip bump connecting the heat sink and the enlarged portion of the emitter.

Claim 22 (previously presented): The power amplifier integrated circuit of claim 21 wherein the flip-chip bump and the heat sink provide an electrical ground connection to the emitter.

Claim 23 (previously presented): A power amplifier integrated circuit comprising:

a substrate;

a transistor disposed on the substrate, the transistor including a collector, a base, and an emitter, the emitter including an enlarged portion located laterally away from the collector and the base;

a heat sink for dissipating heat; and

a via connecting the heat sink and the enlarged portion of the emitter, the via penetrating the substrate at the location of the enlarged portion of the emitter.

Claim 24 (previously presented): The power amplifier integrated circuit of claim 23 wherein the via and the heat sink provide an electrical ground connection to the emitter.

Claim 25 (new): The power amplifier integrated circuit of claim 21 wherein the transistor is integrally formed on the substrate.

Claim 26 (new): The power amplifier integrated circuit of claim 23 wherein the transistor is integrally formed on the substrate.